What is claimed is:

1.   A method for calculating a delay associated with a clock buffer output, said method comprising: calculating the clock buffer output resistance; and using the Elmore Model to calculate the delay taking into account the clock buffer output

5   resistance which has been calculated.

2.   A method as recited in claim 1, further comprising using the Elmore Model to estimate the delay associated with the clock buffer output without taking into account the clock buffer output resistance; and using the estimated delays to calculate

10   the maximum skew error associated with the clock buffer output resistor.

3.   A method as recited in claim 2, using the value of the clock buffer output resistance which has been calculated to calculate the maximum skew error which is associated with the resistance of the clock buffer output.

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4.   A method as recited in claim 1, further comprising using estimated ramp values of a clock buffer input signal and clock buffer output signal to calculate the value of the clock buffer output resistance.

20   5.   A method as recited in claim 4, further comprising using the clock buffer output resistance which has been calculated to calculate the maximum skew error which is associated with the resistance clock buffer output resistance.

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6.   A method for estimating wire delay, said method comprising:

formulating a distributed RC model; calculating an approximate delay based on the

distributed RC model; calculating a capacitance value based on the approximate delay

which has been calculated; and using the capacitance value in the Elmore Model to

5   estimate the wire delay.

7.   A method as recited in claim 6, further comprising calculating a time

domain response relating to the wire.

10   8.   A method as recited in claim 7, using the time domain response which

has been calculated to calculate the approximate delay based on the distributed RC

model.

9.   A method as recited in claim 6, wherein the capacitance value which is

15   calculated is a fraction of a total wire capacitance.

10.   A method as recited in claim 6, further comprising calculating a wire

delay using the Elmore Model without using a distributed RC model.

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11.   A method as recited in claim 10, further comprising calculating clock

skew error using the distributed delay which has been calculated and the wire delay

which has been calculated using the Elmore Model without using a distributed RC

model.

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12.   A method for calculating clock skew error comprising: formulating a

distributed RC model; calculating an approximate delay based on the distributed RC

model; calculating a capacitance value based on the approximate delay which has been

calculated; using the capacitance value in the Elmore Model to estimate the wire

10   delay; and subtracting the wire delay which has been calculated using the Elmore

Model without using a distributed RC model from the distributed delay which has

been calculated in order to calculate clock skew error.

13.   A method as recited in claim 12, further comprising calculating a time

15   domain response relating to the wire.

14.   A method as recited in claim 13, using the time domain response which

has been calculated to calculate the approximate delay based on the distributed RC

model.

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15.   A method as recited in claim 13, wherein the capacitance value which is

calculated is a fraction of a total wire capacitance.

16.   A method as recited in claim 13, further comprising calculating a wire delay using the Elmore Model without using a distributed RC model.

17.   A method as recited in claim 16, further comprising calculating clock skew error using the distributed delay which has been calculated and the wire delay which has been calculated using the Elmore Model without using a distributed RC model.